

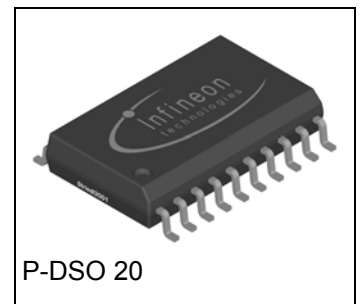
Dual Half Bridge Driver IC

Features

- Compatible to very low ohmic normal level input N-Channel MOSFETs
- Separate input for each MOSFET
- PWM frequency up to 50 kHz
- Operates down to 7.5V supply voltage
- Low EMC sensitivity and emission
- Adjustable dead time with shoot through protection
- Deactivation of dead time and shoot through protection possible
- Short circuit protection for each Mosfet
- Driver undervoltage shut down
- Reverse polarity protection for the driver IC
- Disable function
- Input with TTL characteristics
- 1 bit diagnosis
- Integrated bootstrap diodes

Product Summary

| | | | |
|----------------------|----------------|------------|----|
| Turn on current | $I_{Gxx(on)}$ | 850 | mA |
| Turn off current | $I_{Gxx(off)}$ | 580 | mA |
| Supply voltage range | V_{Vs} | 7.5 ... 60 | V |
| Gate Voltage | V_{GS} | 10 | V |
| Temperature range | T_J | -40...+150 | °C |



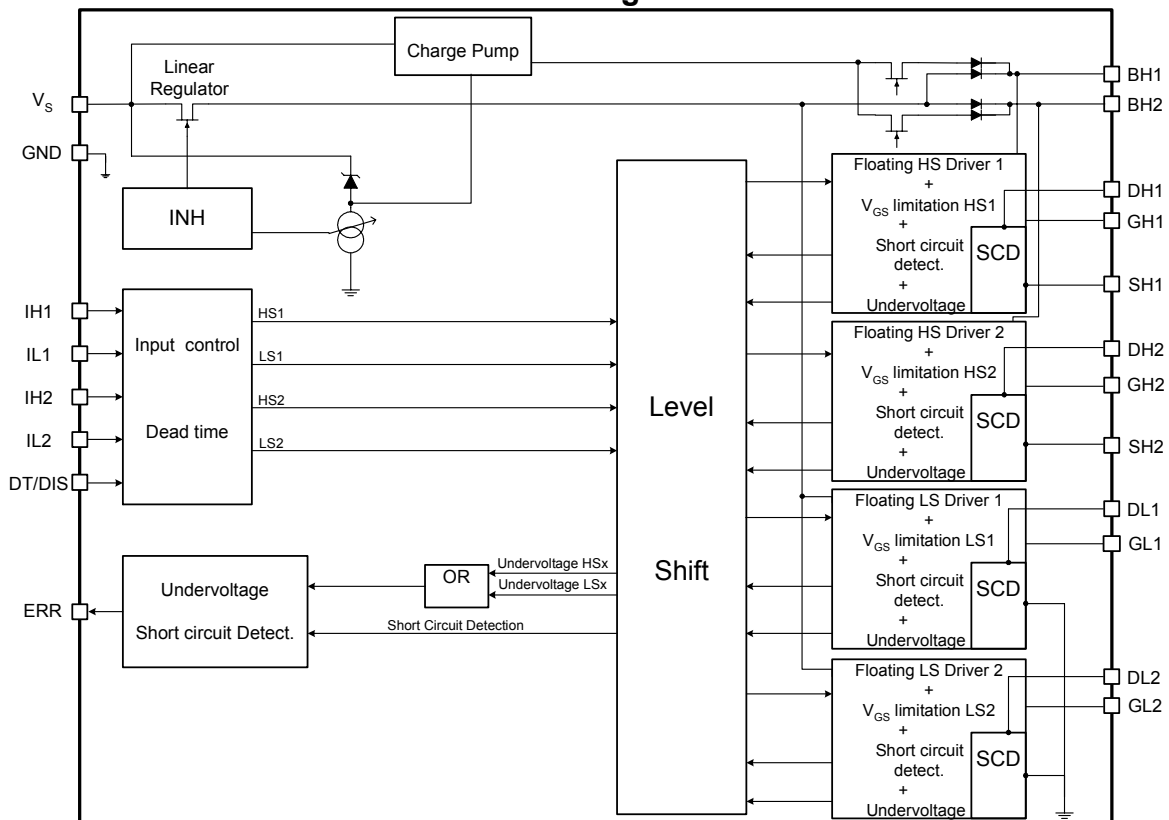
Application

- Dedicated for DC-brush high current motor bridges in PWM control mode and adapted for use in injector and valve applications for 12, 24 and 42V powernet applications. Useable as four fold lowside driver for unipolar 4 phase motor drives.
- The two half bridges can operate independently. The two half bridges can even operate at different supply voltages.

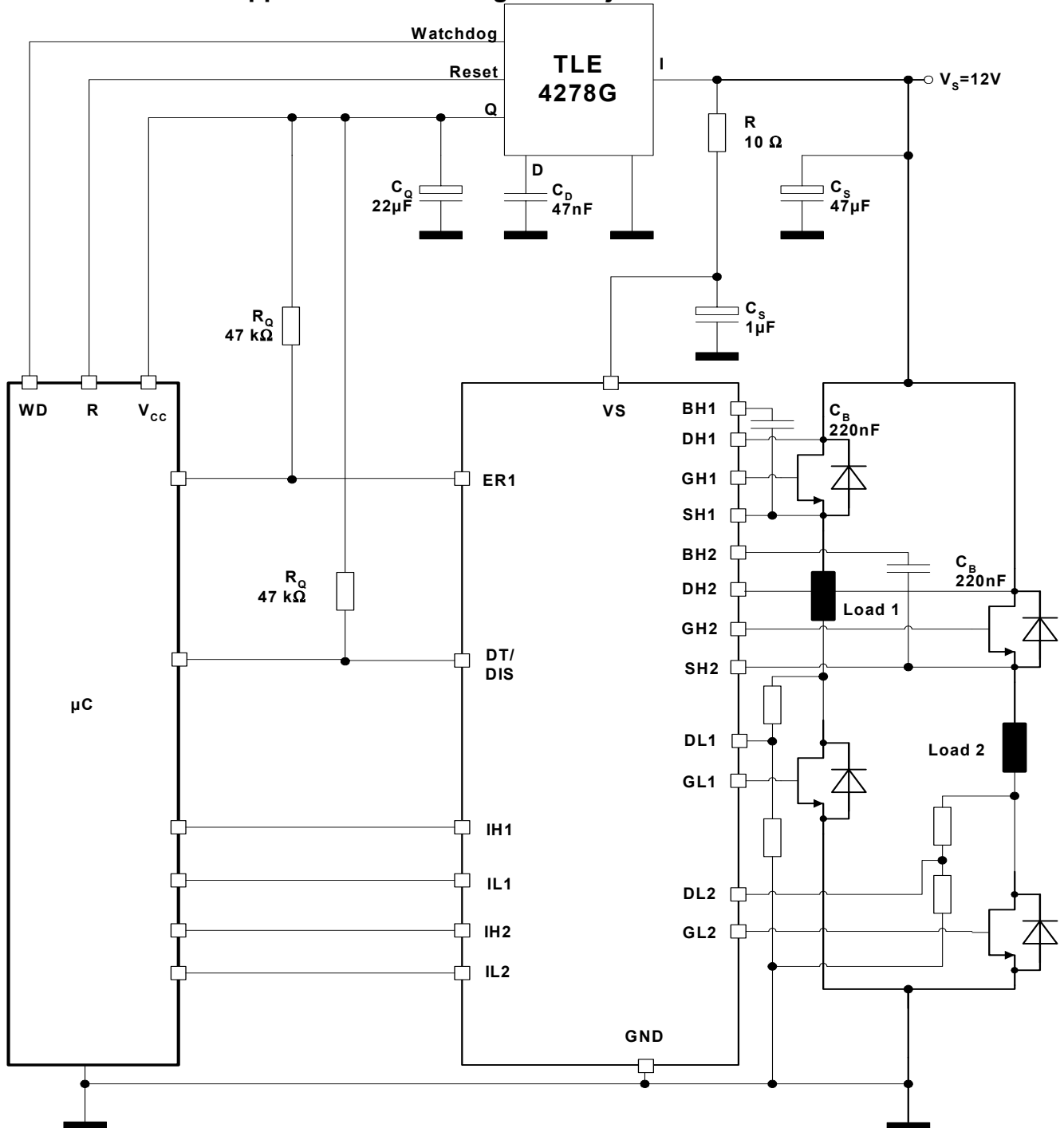
General Description

Dual half bridge driver IC for MOSFET power stages with multiple protection functions.

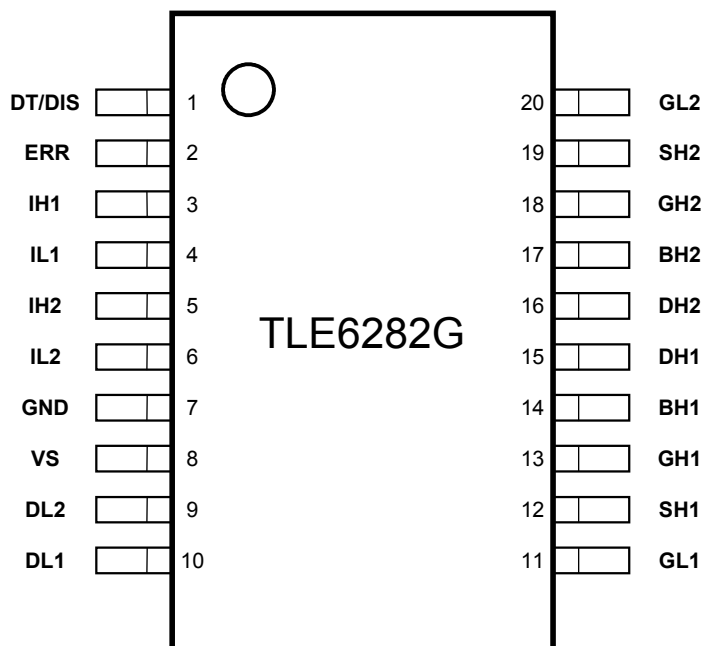
Block Diagram



Application Block Diagram – Injector / Valve Drive



This application diagram shows the principle schematics of a typical injector / valve drive. Other configurations are possible as well. Freewheeling diodes are not considered. The 10 m Ω resistor is not needed by the Driver IC, but may be needed for load current measurement. The voltage divider networks, e.g. $R = 10$ k Ω , across the two Low Side MOSFETs are an example as well; they allow to increase the current limit threshold for Short Circuit protection SCD for the Low Side MOSFETs. As they pull down the Sources of the High Side MOSFETs (while the Low Side MOSFETs are off), they allow to pre-charge the C_{BX} capacitors during start-up (before the Driver IC gets enabled). The SCD current limit threshold can be increased for the High Side MOSFETs as well by using voltage divider networks across the High Side MOSFETs. SCD can also be disabled (High Side and / or Low Side MOSFETs).



| Pin | Symbol | Function |
|-----|--------|--|
| 1 | DT/DIS | a) Set adjustable dead time by external resistor b) Deactivate deadtime and shoot through protection by connecting to 0V c) Reset ERR register d) Disable output stages |
| 2 | ERR | Error flag for driver shut down |
| 3 | IH1 | Control input for high side switch 1 |
| 4 | IL1 | Control input for low side switch 1 |
| 5 | IH2 | Control input for high side switch 2 |
| 6 | IL2 | Control input for low side switch 1 |
| 7 | GND | Ground |
| 8 | VS | Voltage supply |
| 9 | DL2 | Sense contact for short circuit detection low side 2 |
| 10 | DL1 | Sense contact for short circuit detection low side 1 |
| 11 | GL1 | Output to gate low side switch 1 |
| 12 | SH1 | Connection to source high side switch 1 |
| 13 | GH1 | Output to gate high side switch 1 |
| 14 | BH1 | Bootstrap supply high side switch 1 |
| 15 | DH1 | Sense contacts for short circuit detection high side 1 |
| 16 | DH2 | Sense contacts for short circuit detection high side 2 |
| 17 | BH2 | Bootstrap supply high side switch 2 |
| 18 | GH2 | Output to gate high side switch 2 |
| 19 | SH2 | Connection to source high side switch 2 |
| 20 | GL2 | Output to gate low side switch 2 |

Maximum Ratings at $T_j = -40 \dots +150^\circ\text{C}$ unless specified otherwise

| Parameter | Symbol | Limits Values | | Unit |
|--|-----------------------------------|---------------|------|------------------|
| Supply voltage ¹ | V_S | -4 | 60 | V |
| Operating temperature range | T_j | -40 | 150 | $^\circ\text{C}$ |
| Storage temperature range | T_{stg} | -55 | 150 | |
| Max. voltage range at lxx; DT/DIS | | -1 | 6 | V |
| Max. voltage range at ERR | | -0.3 | 6 | V |
| Max. voltage range at BHx | V_{BHx} | -0.3 | 90 | V |
| Max. voltage range at DHx ² | V_{DHx} | -4 | 75 | V |
| Max. voltage range at GHx ³ | V_{GHx} | -7 | 86 | V |
| Max. voltage range at SHx ³ | V_{SHx} | -7 | 75 | V |
| Max. voltage range at DLx | V_{DLx} | -7 | 75 | V |
| Max. voltage range at GLx | V_{GLx} | -2 | 12 | V |
| Max. voltage difference BHx - SHx | $V_{\text{BHx}} - V_{\text{SHx}}$ | -0.3 | 17 | V |
| Max. voltage difference GHx – SHx; GLx | $V_{\text{Gxx}} - V_{\text{Sxx}}$ | -0.3 | 11 | V |
| Power dissipation (DC) @ $T_A = 125^\circ\text{C}$ / min. footprint | P_{tot} | | 0.33 | W |
| Power dissipation (DC) @ $T_A = 85^\circ\text{C}$ / min. footprint | P_{tot} | | 0.85 | W |
| Electrostatic discharge voltage (Human Body Model) according to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 – 1993 | V_{ESD}^4 | | 2 | kV |
| Jedec Level | | | 3 | |
| Thermal resistance junction - ambient (minimal footprint with thermal vias) | R_{thJA} | | 75 | K/W |
| Thermal resistance junction - ambient (6 cm ²) | R_{thJA} | | 75 | K/W |

Functional range

| Parameter and Conditions at $T_j = -40 \dots +150^\circ\text{C}$, unless otherwise specified | Symbol | Values | | Unit |
|--|------------------|--------|-----|------------------|
| | | | | |
| Supply voltage | V_S | 7.5 | 60 | V |
| Operating temperature range | T_j | -40 | 150 | $^\circ\text{C}$ |
| Max. voltage range at lxx, DT/DIS | | -0.3 | 5.5 | V |
| Max. voltage range at ERR | | -0.3 | 5.5 | V |
| Max. voltage range at BHx | V_{BHx} | -0.3 | 90 | V |
| Max. voltage range at DHx ² | V_{DHx} | -4 | 75 | V |
| Max. voltage range at GHx ³ | V_{GHx} | -7 | 86 | V |
| Max. voltage range at SHx ³ | V_{SHx} | -7 | 75 | V |

¹ With external resistor ($\geq 10 \Omega$) and capacitor

² The min value -4V is increased to $-(V_{\text{BHx}} - V_{\text{SHx}})$ in case of bootstrap voltages <4V

³ The min value -7V is reduced to $-(V_{\text{BHx}} - V_{\text{SHx}} - 1\text{V})$ in case of bootstrap voltages <8V

⁴ All test involving Gxx pins $V_{\text{ESD}} = 1 \text{ kV!}$

| | | | | |
|---|---------------------|------|----|---------|
| Max. voltage range at DLx ³ | V_{DLx} | -7 | 75 | V |
| Max. voltage range at GLx | V_{GLx} | -2 | 12 | V |
| Max. voltage difference BHx - SHx | $V_{BHx} - V_{SHx}$ | -0.3 | 12 | V |
| Max. voltage difference GHx - SHx; GLx | $V_{Gxx} - V_{Sxx}$ | -0.3 | 11 | V |
| PWM frequency | F_{PWM} | 0 | 50 | kHz |
| Minimum on time external lowside switch – static condition @ 20 kHz; $Q_{Gate} = 200nC$ | $t_{p(min)}$ | | 2 | μs |

Electrical Characteristics

| Parameter and Conditions at $T_j = -40...+150\text{ }^{\circ}C$, unless otherwise specified and supply voltage range $V_S = 7.5 \dots 60V$; $f_{PWM} = 20kHz$ | Symbol | Values | | | Unit |
|---|--------|--------|-----|-----|------|
| | | min | typ | max | |

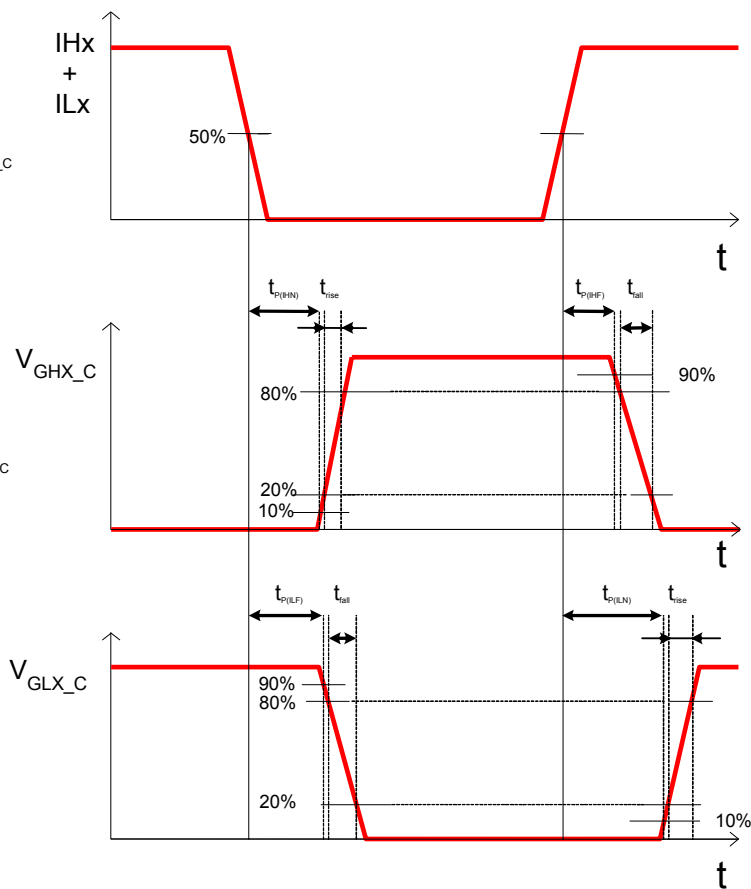
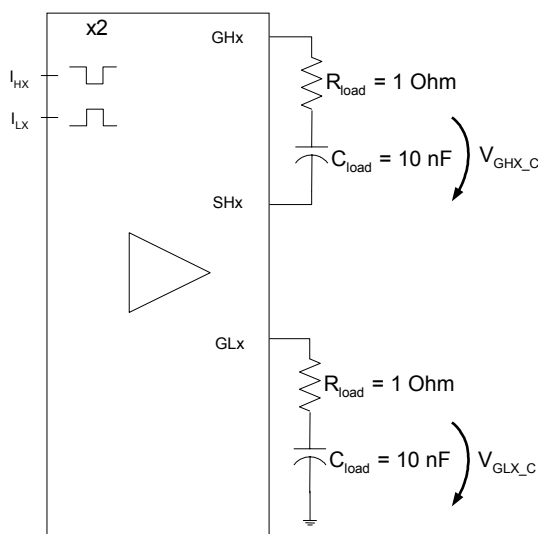
Static Characteristics

| | | | | | |
|--|-------------------|-----|-----|-----|----|
| Low level output voltage (V_{GSxx}) @ $I = 10mA$ | ΔV_{LL} | -- | 60 | 150 | mV |
| High level output voltage (V_{GSxx}) @ $I = -10mA$; $V_S > 12V$ | ΔV_{HL} | 8 | 10 | 11 | V |
| Supply current at V_S (device disabled) @ $V_{bat} = V_S = 14V$ $R_{DT} = 400k\Omega$ | $I_{VS(dis)14V}$ | -- | 4 | 8 | mA |
| Supply current at V_S (device disabled) @ $V_{bat} = V_S = 42V$ $R_{DT} = 400k\Omega$ | $I_{VS(dis)42V}$ | -- | 4 | 8 | mA |
| Supply current at V_S @ $V_{bat} = V_S = 14V$ 20kHz (Outputs open) | $I_{VS(open)14V}$ | -- | 7 | 15 | mA |
| Supply current at V_S @ $V_{bat} = V_S = 14V$ 50kHz (Outputs open) | $I_{VS(open)14V}$ | -- | 7 | 15 | mA |
| Supply current at V_S @ $V_{bat} = V_S = 42V$ 20kHz (Outputs open) | $I_{VS(open)42V}$ | -- | 7 | 15 | mA |
| Low level input voltage | $V_{IN(LL)}$ | -- | -- | 1.0 | V |
| High level input voltage | $V_{IN(HL)}$ | 2.0 | -- | -- | V |
| Input hysteresis | ΔV_{IN} | 100 | 170 | | mV |

Dynamic characteristics (pls. see test circuit and timing diagram)

| | | | | | |
|---|----------------|--------------------------|-------------------------|--------------------------|---------|
| Turn on current @ $V_{Gxx} - V_{Sxx} = 0V$; $T_j = 25^\circ C$ @ $V_{Gxx} - V_{Sxx} = 4V$; $T_j = 125^\circ C$ @ $C_{Load} = 22nF$; $R_{Load} = 0\Omega$ | $I_{Gxx(on)}$ | -- -- | 850 700 | -- -- | mA |
| Turn off current @ $V_{Gxx} - V_{Sxx} = 10V$; $T_j = 25^\circ C$ @ $V_{Gxx} - V_{Sxx} = 4V$; $T_j = 125^\circ C$ @ $C_{Load} = 22nF$; $R_{Load} = 0\Omega$ | $I_{Gxx(off)}$ | -- -- | 580 300 | -- -- | mA |
| Dead time (adjustable) @ $R_{DT} = 1 k\Omega$ @ $R_{DT} = 10 k\Omega$ @ $R_{DT} = 50 k\Omega$ @ $R_{DT} = 200 k\Omega$ @ $C_{Load} = 10nF$; $R_{Load} = 1\Omega$ | t_{DT} | -- 0.05 0.40 -- | 0 0.24 1.0 3.1 | -- 0.38 2.50 -- | μs |
| Rise time @ $C_{Load} = 10nF$; $R_{Load} = 1\Omega$ (20% to 80%) | t_{rise} | -- | 100 | 300 | ns |
| Fall time @ $C_{Load} = 10nF$; $R_{Load} = 1\Omega$ (80% to 20%) | t_{fall} | -- | 150 | 440 | ns |
| Disable propagation time @ $C_{Load} = 10nF$; $R_{Load} = 1\Omega$ | $t_{P(DIS)}$ | 3.4 | 5 | 7 | μs |
| Reset time of diagnosis @ $C_{Load} = 10nF$; $R_{Load} = 1\Omega$ | $t_{P(CL)}$ | 1 | 2 | 3.1 | μs |
| Input propagation time (low side turns on, 0% to 10%) | $t_{P(ILN)}$ | -- | 160 | 500 | ns |
| Input propagation time (low side turns off, 100% to 90%) | $t_{P(ILF)}$ | -- | 100 | 500 | ns |
| Input propagation time (high side turns on, 0% to 10%) | $t_{P(IHN)}$ | -- | 120 | 500 | ns |
| Input propagation time (high side turns off, 100% to 90%) | $t_{P(IHF)}$ | -- | 120 | 500 | ns |
| Input propagation time difference (all channels turn on) | $t_{P(Diff)}$ | 20 | 40 | 70 | ns |
| Input propagation time difference (all channels turn off) | $t_{P(Diff)}$ | -- | 20 | 50 | ns |
| Input propagation time difference (one channel; low on – high off) | $t_{P(Diff)}$ | -- | 40 | 150 | ns |
| Input propagation time difference (one channel; high on – low off) | $t_{P(Diff)}$ | -- | 20 | 150 | ns |
| Input propagation time difference (all channels; low on – high off) | $t_{P(Diff)}$ | -- | 40 | 150 | ns |
| Input propagation time difference (all channels; high on – low off) | $t_{P(Diff)}$ | -- | 20 | 150 | ns |

Test Circuit and Timing Diagram



Test Conditions :

Junction temperature $T_j = -40 \dots 150^\circ\text{C}$

Supply voltage range $V_s = 7.5 \dots 60\text{V}$

PWM frequency $f_{PWM} = 20 \text{ kHz}$

Diagnosis and Protection Functions

| | | | | | |
|--|------------------|------|------|------|---------------|
| Short circuit protection filter time | $t_{SCP(off)}$ | 6 | 9 | 12 | μs |
| Short circuit criteria (V_{DS} of Mosfets) | $V_{DS(SCP)}$ | | | | |
| For Low Sides | | 0.5 | 0.75 | 1.0 | V |
| For High Sides | | 0.45 | 0.75 | 1.05 | V |
| Disable input level | V_{DIS} | 3.3 | 3.7 | 4.0 | V |
| Disable input hysteresis | ΔV_{DIS} | | 180 | | mV |
| Deactivation level for dead time and shoot through protection | V_{DIS} | 0.6 | 0.85 | 1.1 | V |
| Deactivation input hysteresis | ΔV_{DIS} | | 170 | | mV |
| Error level @ 1.6mA I_{ERR} | V_{ERR} | -- | -- | 1.0 | V |
| Under voltage lock out for highside output – bootstrap voltage | $V_{BHx(uvlo)}$ | | 3.7 | 4.6 | V |
| Under voltage lock out for lowside output – supply voltage | $V_{Vs(uvlo)}$ | | 4.8 | 5.9 | V |

Remarks:

Default status of input pins:

To assure a defined status of all input pins in case of disconnection, these pins are internally secured by pull up / pull down current sources with approx. 20 μ A.

The following table shows the default status of each input pin.

| Input pin | Default status |
|----------------------|----------------|
| ILx (active high) | Low |
| IHx (active low) | High |
| DT/DIS (active high) | High |

Definition:

In this datasheet a duty cycle of 98% means that the GLx pin is 2% of the PWM period in high condition.

Functional description

Description of Dead Time Pin / Disable Pin / Reset

In the range between 1.5 and 3.5 V the dead time is varied from 100ns to 3.1 μ s typ. In the range below 1.0V the dead time is disabled / shoot through is allowed. Both external Mosfets of the same half bridge can be switched on simultaneously. This function allows the use of a half bridge for valves and injectors. In the range above 4.0V the device is disabled.

If DIS is pulled up to 5V for 3.1 to 3.4 μ s only the ERR register is cleared (reset), no output stage is shut down. A shut down of all external Mosfets occurs if DIS is pulled up for longer than 7 μ s.

| Condition of DT/DIS pin | Function |
|-------------------------|---|
| 0 - 1V | Disable of dead time; Shoot through is allowed |
| 1.5 - 3.5V | Adjust dead time between 100ns and 3.1 μ s typ. |
| > 4V | a) Reset of diagnosis register if DT/DIS voltage is higher than 4V for a time between 3.1 μ s and 3.4 μ s |
| | b) Shut down of output stages if DT/DIS voltage is higher than 4V for a time above 7 μ s (Active pull down of gate voltage) |

Description of Diagnosis

The ERR pin is an open collector output and has to be pulled up with external pull up resistors to 5V. In normal conditions the ERR signal is high. In case of shutdown of any output stage the ERR is pulled down. This shut down can be caused by undervoltage or short circuit.

Recommended Start-up procedure

The following procedure is recommended whenever the Driver IC is powered up:

- Disable the Driver IC via DT/DIS pin
- After the supply voltage has ramped up, wait for several ms to pre-charge the bootstrap capacitors of the High Side MOSFETs C_{Bx} through the resistors R on the DLx

pins (voltage divider network, pls. see Application block diagram on pg. 2)

$t_{WAIT} \approx 3 \times C_{BX} \times 2 \times R$, whereas $R = 10 \text{ k}\Omega$

- Enable the Driver IC via DT/DIS pin
- Start the operation by applying the desired pulse patterns. Do not apply any pulse patterns to the IHx or ILx pins, before the C_{BX} capacitors are charged up.

Alternatively, the Driver IC can be enabled via the DT/DIS pin right after ramping up the supply voltage V_S . Now, the two Low Side MOSFETs are turned on via the ILx control inputs (to pull down the Sources of the High Side MOSFETs and to charge up the bootstrap capacitors C_{BX} within several $10 \mu\text{s}$). The regular operation can be started when the bootstrap capacitors are charged up.

Short Circuit protection

The current threshold limit to activate the Short Circuit protection function can be adjusted to larger values, it can not be adjusted to lower values. This can be done by external resistors to form voltage dividers across the “sense element” (pls. see Application block diagram on pg. 2), consisting of the Drain-Source-Terminals, a fraction of the PCB trace and – in some cases – current sense resistors (used by the μC not by the Driver IC).

The Short Circuit protection can be disabled for the High Side MOSFETs by shorting DH1 with SH1 and DH2 with SH2 on the PCB; in this case the DHx pins may not be connected to the Drains of the associated MOSFETs. To disable Short Circuit protection for the Low Side MOSFETs the DL1 and DL2 pin should be connected to the Driver IC’s Ground.

Shut down of the driver

A shut down can be caused by undervoltage or short circuit.

A short circuit will shut down only the affected Mosfet until a reset of the error register by a disable of the driver occurs. A shut down due to short circuit will occur only when the Short Circuit criteria $V_{DS(SCP)}$ is met for a duration equal to or longer than the Short Circuit filter time $t_{SCP(off)}$. Yet, the exposure to or above $V_{DS(SCP)}$ is not counted or accumulated. Hence, repetitive Short Circuit conditions shorter than $t_{SCP(off)}$ will not result in a shut down of the affected MOSFET.

An undervoltage shut down shuts only the affected output down. The affected output will auto restart after the undervoltage situation is over.

Operation at $V_S < 12\text{V}$

If $V_S < 11.5\text{V}$ the gate voltage will not reach 10V . It will reach approx. $V_S - 1.5\text{V}$, dependent on duty cycle, total gate charge and switching frequency.

Operation at different voltages for V_S , DH1 and DH2

If DH1 and DH2 are used with a voltage higher than V_S , a duty cycle of 100% can not be guaranteed. In this case the driver is acting like a normal driver IC based on the bootstrap principle. This means that after a maximum “On” time of the highside switch of more than 1ms a refresh pulse to charge the bootstrap capacitor of about $1\mu\text{s}$ is needed to avoid undervoltage lock out of this output stage.

Operation at extreme duty cycle:

The integrated charge pump allows an operation at 100% duty cycle. The charge pump is strong enough to replace leakage currents during “on”-phase of the highside switch. The gate charge for fast switching of the highside switches is supplied by the bootstrap capacitors. This means, that the bootstrap capacitor needs a minimum charging time of about $1\mu\text{s}$, if the highside switch is operated in PWM mode (e.g. with 20kHz a maximum duty cycle of 96% can be reached). The exact value for the upper limit is given by the RC time formed by

the impedance of the internal bootstrap diode and the capacitor formed by the external Mosfet ($C_{\text{Mosfet}} = Q_{\text{Gate}} / V_{\text{GS}}$). The size of the bootstrap capacitor has to be adapted to the external MOSFET the driver IC has to drive. Usually the bootstrap capacitor is about 10-20 times bigger then C_{Mosfet} . External components at the Vs Pin have to be considered, too.

General remark:

It is assured that after the removal of any fault condition, which did not damage the device, the device will return to normal conditions without external trigger. Only short circuit condition needs restart by reset.

Estimation of power loss within the Driver IC

The power loss within the Driver IC is strongly dependent on the use of the driver and the external components. Nevertheless a rough estimation of the worst case power loss is possible.

Worst case calculation is:

$$P_{\text{Loss}} = (Q_{\text{gate}} * n * \text{const} * f_{\text{PWM}} + I_{\text{VS(open)}} / 20\text{kHz}) * V_{\text{Vs}} - P_{\text{RGate}}$$

With:

P_{Loss} = Power loss within the Driver IC

f_{PWM} = Switching frequency

Q_{gate} = Total gate charge of used MOSFETs at 10V V_{GS}

n = Number of switched MOSFETs

const = Constant considering some leakage current in the driver (about 1.2)

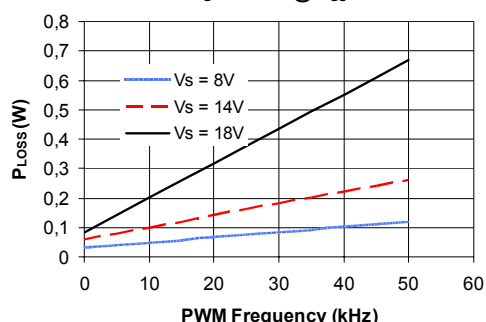
$I_{\text{VS(open)}}$ = Current consumption of driver without connected Mosfets during switching

V_{Vs} = Voltage at Vs

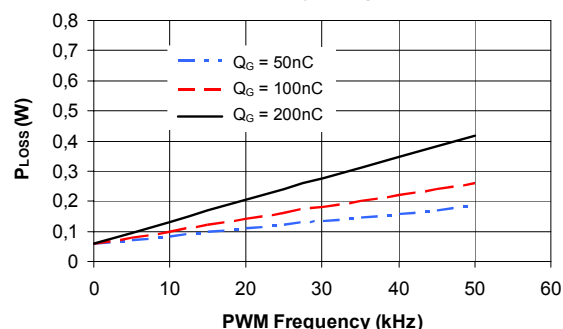
P_{RGate} = Power dissipation in the external gate resistors

This value can be reduced dramatically by usage of external gate resistors.

Estimated Power Loss P_{Loss} within the Driver IC
for different supply voltages V_{s}
at $Q_{\text{G}} = 100\text{nC}$ @ $V_{\text{GS}} = 10\text{V}$



Estimated Power Loss P_{Loss} within the Driver IC
for different gate charges Q_{G}
at supply voltage $V_{\text{s}} = 14\text{V}$



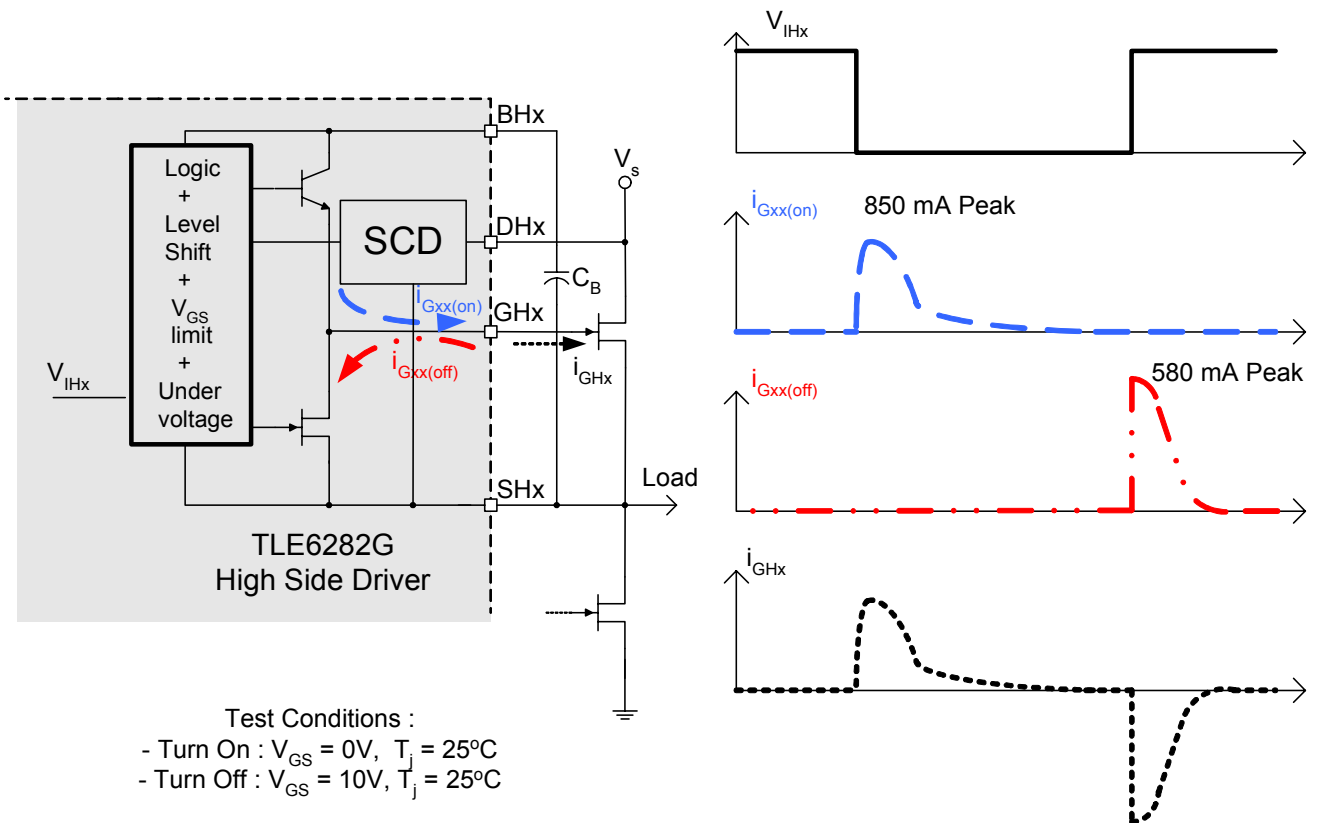
Conditions :

Junction temperature $T_{\text{j}} = 25^{\circ}\text{C}$

Number of switched MOSFET $n = 2$

Power dissipation in the external gate resistors $P_{\text{RGate}} = 0,2 * P_{\text{Loss}}$

Gate Drive characteristics



This figure represents the simplified internal circuit of one high side gate drive. The drive circuit of the low sides looks similar.

This figure illustrates typical voltage and current waveforms of the high side gate drive; the associated waveforms of the low side drives look similar.

Truth Table

| Input | | | Conditions | | Output | | |
|-------|-----|----------|------------|----|--------|-----|-----|
| ILx | IHx | DT / DIS | UV | SC | GLx | GHx | ERR |
| 1 | 1 | <3.5V | 0 | 0 | 1 | 0 | 5V |
| 0 | 0 | <3.5V | 0 | 0 | 0 | 1 | 5V |
| 1 | 0 | 1.5-3.5V | 0 | 0 | A | A | 5V |
| 1 | 0 | <1V | 0 | 0 | 1 | 1 | 5V |
| 0 | 1 | <3.5V | 0 | 0 | 0 | 0 | 5V |
| 1 | 1 | <3.5V | 1 | 0 | B | 0 | C |
| 0 | 0 | <3.5V | 1 | 0 | 0 | B | C |
| 1 | 0 | 1.5-3.5V | 1 | 0 | D | D | C |
| 1 | 0 | <1V | 1 | 0 | B | B | C |
| 0 | 1 | <3.5V | 1 | 0 | 0 | 0 | C |
| 1 | 1 | <3.5V | 0 | 1 | E | 0 | F |
| 0 | 0 | <3.5V | 0 | 1 | 0 | E | F |
| 1 | 0 | 1.5-3.5V | 0 | 1 | D | D | F |
| 1 | 0 | <1V | 0 | 1 | E | E | F |
| 0 | 1 | <3.5V | 0 | 1 | 0 | 0 | F |
| X | X | X | X | X | 0 | 0 | 5V |
| X | X | >4V | X | X | 0 | 0 | 5V |

- A) stays in the condition before the shoot through command occurs (see also dead time diagrams)
- B) 0 when affected; 1 when not affected; self recovery
- C) 0V when output does not correspond to input patterns; 5V when output corresponds to input patterns.
- D) stays in the condition before the shoot through command occurs (see also dead time diagrams); 0 when affected
- E) 0 when affected– the outputs of the affected halfbridge are shut down and stay latched until reset; 1 when not affected
- F) 0V when output does not correspond to input patterns – the outputs of the affected half-bridge are shut down and stay latched until reset; 5V when output corresponds to input patterns.
- X) Condition has no influence

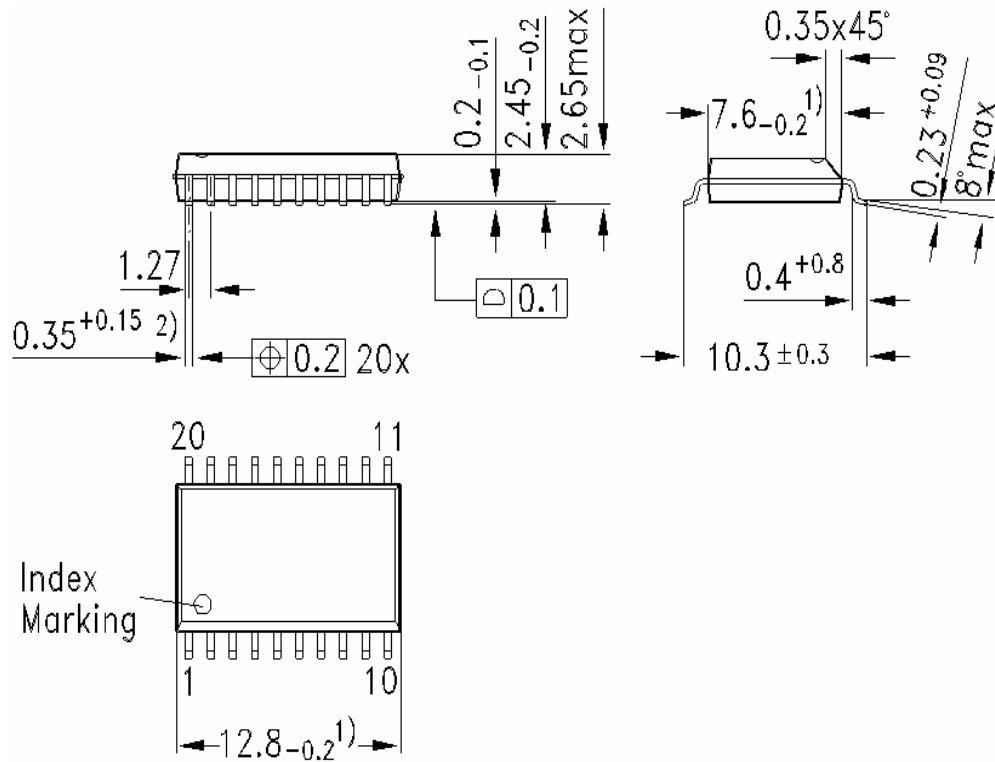
Remark: Please consider the influence of the dead time for your input duty cycle

Package and Ordering Code

(all dimensions in mm)

Package Code

P-DSO 20



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